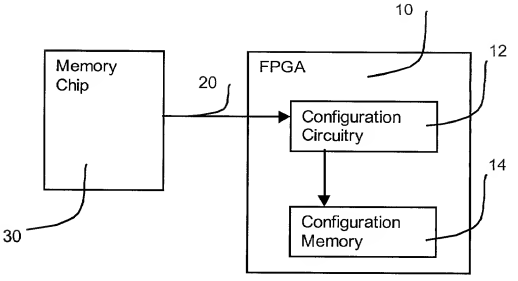

Figure 1 PRIOR ART

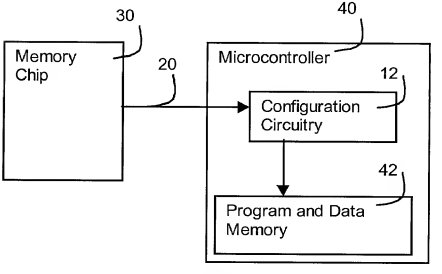

Figure 2 PRIOR ART

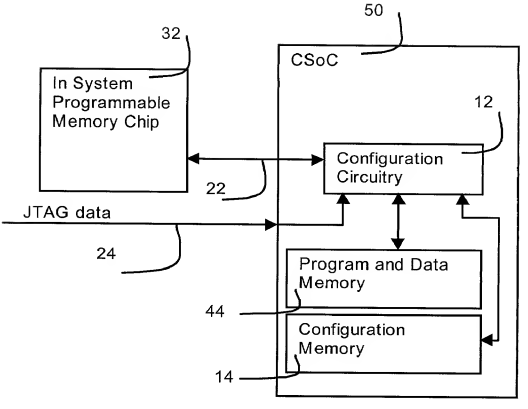

Figure 3 PRIOR ART

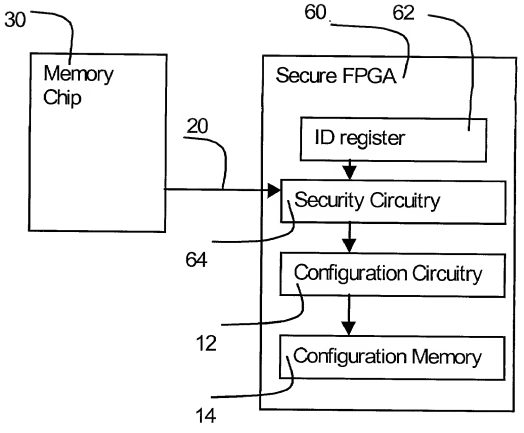

Figure 4 PRIOR ART

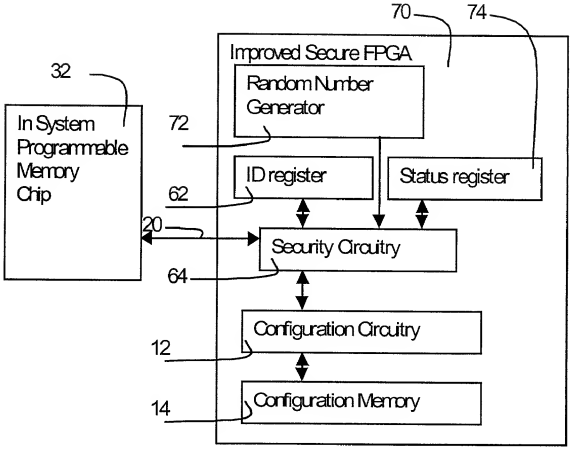
70
74
Improved Secure FPGA
32
Random Number Generator
In System Programmable Memory Chip
72
ID register
Status register
62
20
Security Circuitry
64
Configuration Circuitry
12
Configuration Memory
14

Figure 5

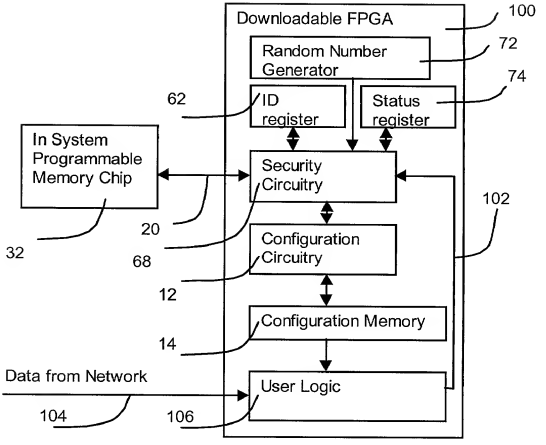
Downloadable FPGA
100
Random Number Generator
72
74
62
ID register
Status register
In System Programmable Memory Chip
Security Circuitry
102
20
32
Configuration Circuitry
68
12
Configuration Memory
14
Data from Network
User Logic
104
106

Figure 6

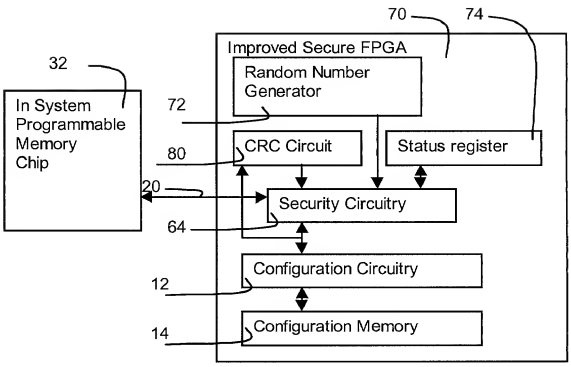
70
74
Improved Secure FPGA
Random Number Generator
32
In System Programmable Memory Chip
72
80
CRC Circuit
Status register
20
Security Circuitry
64
Configuration Circuitry
12
Configuration Memory
14

Figure 7